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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/620,649	07/20/00	KAYA C	TI-23686.I

MMC1/0409

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EXAMINER	
GOODWIN.D	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 04/09/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/620,649	KAYA, CETIN NMI	
	Examiner	Art Unit	
	David Goodwin	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-19* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☒ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other:

DETAILED ACTION

This office action is in response to the instant application filed on July 20, 2000.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1 through 11, drawn to a method of making a semiconductor device, classified in class 438, subclass 257.

II. Claims 12 though 20, drawn to a semiconductor device, classified in class 257, subclass 332.

The inventions are distinct, each from the other because:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the gate structures could be fbricated using a dummy gate process.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with J. Kantor on February 13, 2001 a provisional election was made without traverse to prosecute the invention of a semiconductor device, claims 12 through 20. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1 through 11 withdrawn from further

consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

The draftsperson has approved of the drawings.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 12, 13, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Buskirk (US patent 6,001,689).

Van Buskirk teaches an integrated circuit comprising a floating gate memory array. Wherein the array comprises a plurality of gate stacks having a channel dielectric (61), a polysilicon floating gate (51), a floating gate dielectric (71), and a polysilicon gate electrode (41) (column 4 lines 1-10). The structure further comprises trenches and moats (fig 7A) formed between the stacks (column 5 lines 35-55). First oxide spacers

(121) and oxide layer (101) are formed between the stacks and subsequently planarized to expose the polysilicon gate electrode (41) (column 5 lines 35-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk (US patent 6,001,689) in view of Woo (US patent 5,926,711).

Van Buskirk teaches all aspects of the claimed invention above. However, Van Buskirk does not teach the use of hemispherical grained silicon on the floating gate.

Woo teaches a floating gate transistor wherein the floating gate (24C) is formed of amorphous silicon which is converted to hemispherical grains of silicon (fig 3f, column 4 lines 35-55).

It would have been obvious to one of ordinary skill in the art to use a floating gate having hemispherical grains of silicon in order to improve the capacitive coupling of the floating and control gates.

Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk (US patent 6,001,689) in view of Chan (US patent 6,051,467).

Van Buskirk teaches all aspects of the claimed invention above. However, Van Buskirk does not teach the thickness of the oxide layer in the ONO intergate dielectric.

Chan teaches that a typical thickness for the oxide layer in an ONO intergate dielectric is between 50 and 100 angstroms (column 3 lines 40-50).

It would have been obvious to one of ordinary skill in the art to use an oxide with a thickness of between 50 and 100 angstroms in an ONO intergate dielectric order to provide sufficient gate separation and capacitative coupling.

Further it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed dielectric isolation dielectric thickness limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another isolation dielectric thickness. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

Allowable Subject Matter

Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach or suggest a semiconductor device comprising a plurality of floating gate stacks with dielectric isolation regions, a peripheral dielectric disposed outwardly from the floating gate stacks and a peripheral region of the substrate, and at least one peripheral gate disposed outwardly from the peripheral region of the substrate.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Thakur (5658381), Wu (6008090), Doan (5767005), Wu (6084265), Wu (6117756). Nishimoto (5814543), Fugiwara (5898197), Mine (6144062), Wu (5998264), Thakur (5837580), and Yew (5753559) teach relevant floating gate structures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Goodwin whose telephone number is (703)308-4931. The examiner can normally be reached on Mon-Fri from 9:00am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (703)308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-2774.

DJG
March 23, 2001

Mary Wilczewski
Primary Examiner